

FIG. 1

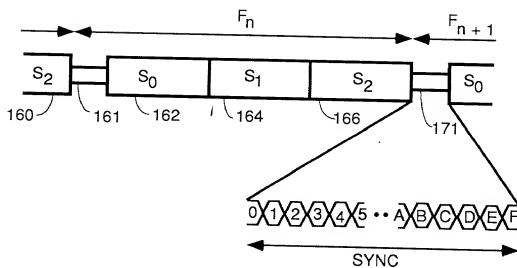


FIG. 2A

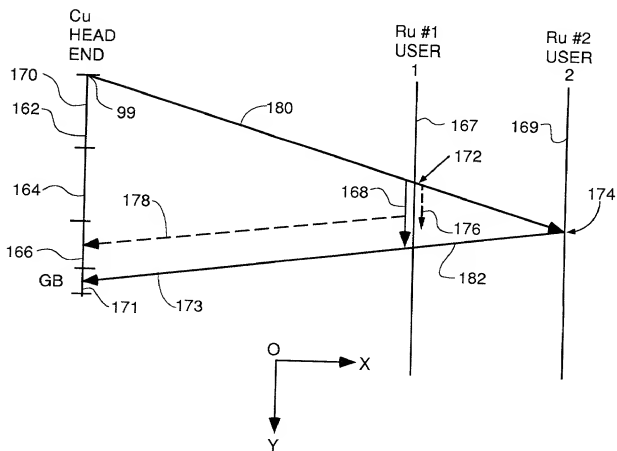
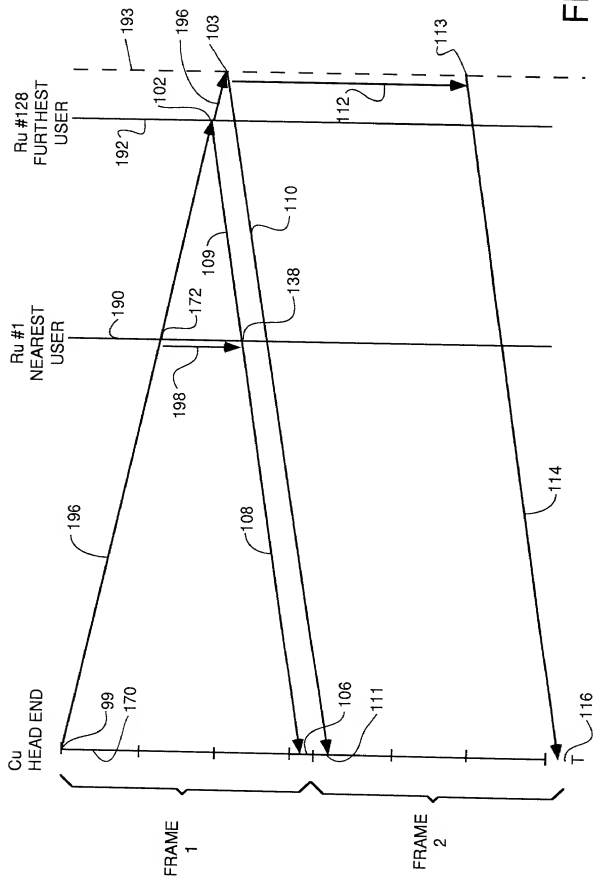
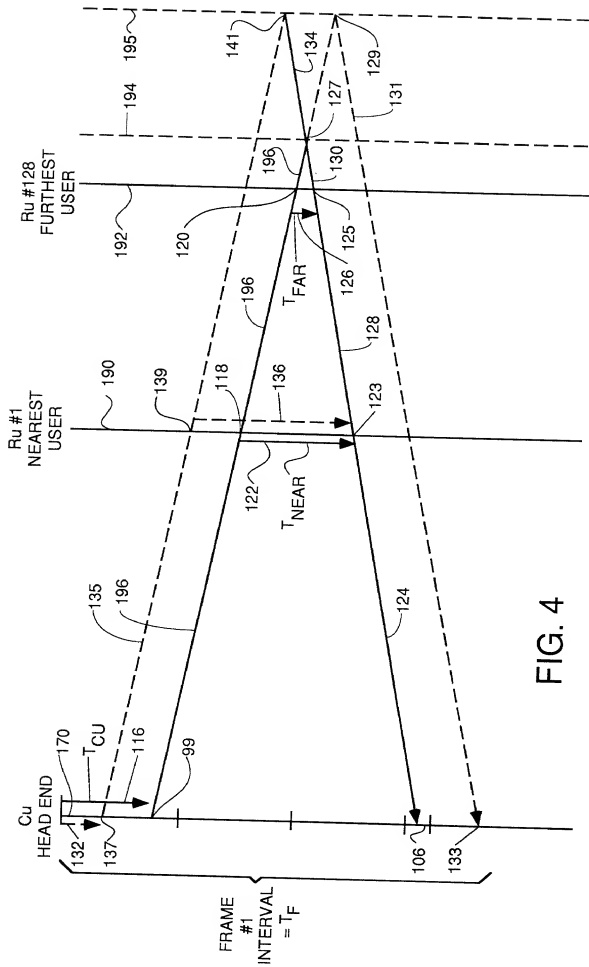


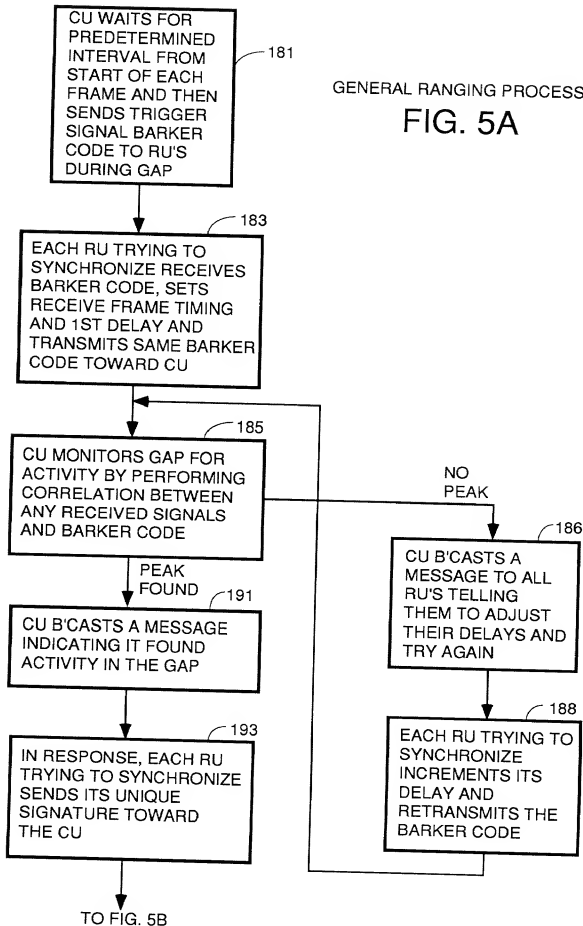
FIG. 2B





GENERAL RANGING PROCESS

FIG. 5A



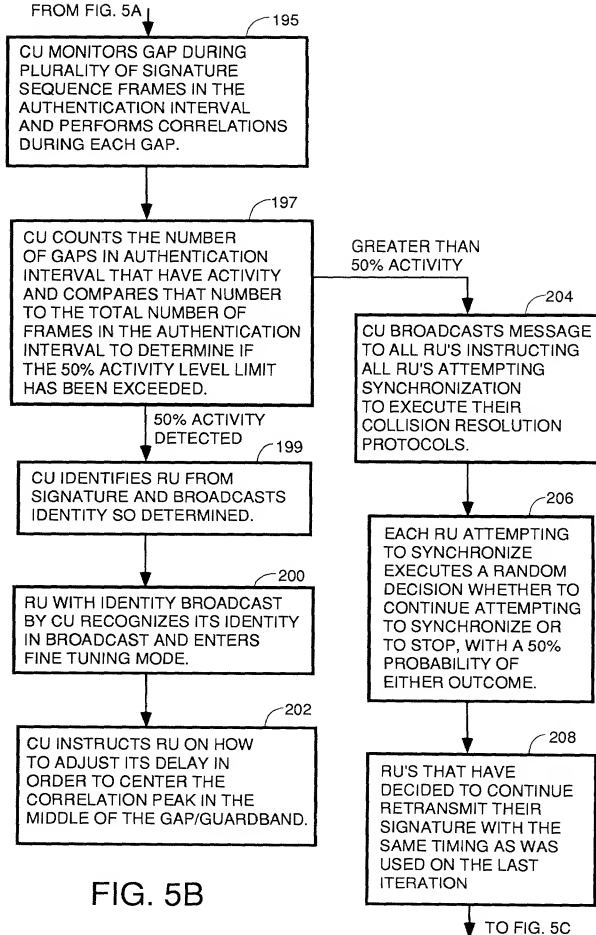


FIG. 5B

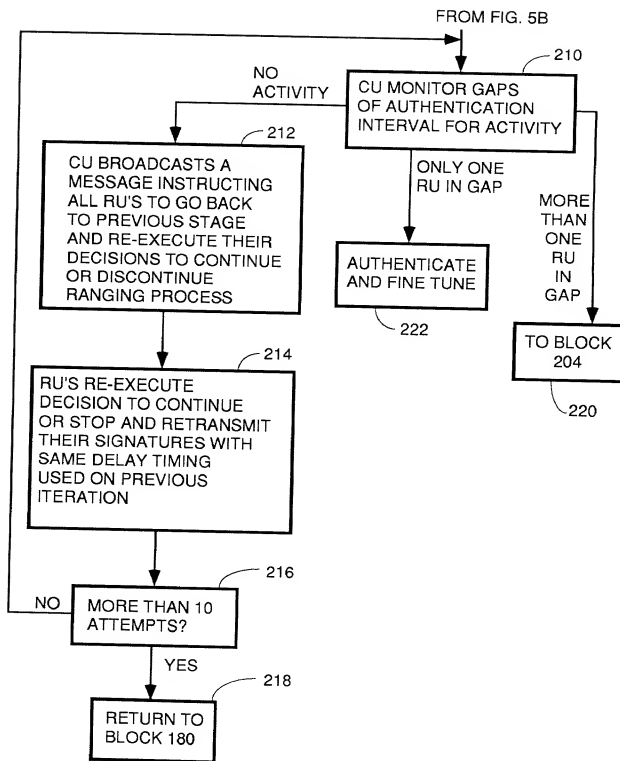


FIG. 5C

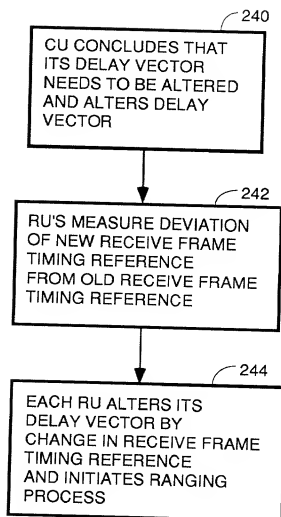


FIG. 6
DEAD RECKONING RE-SYNC

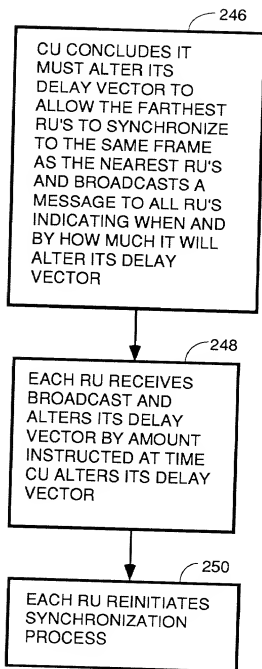
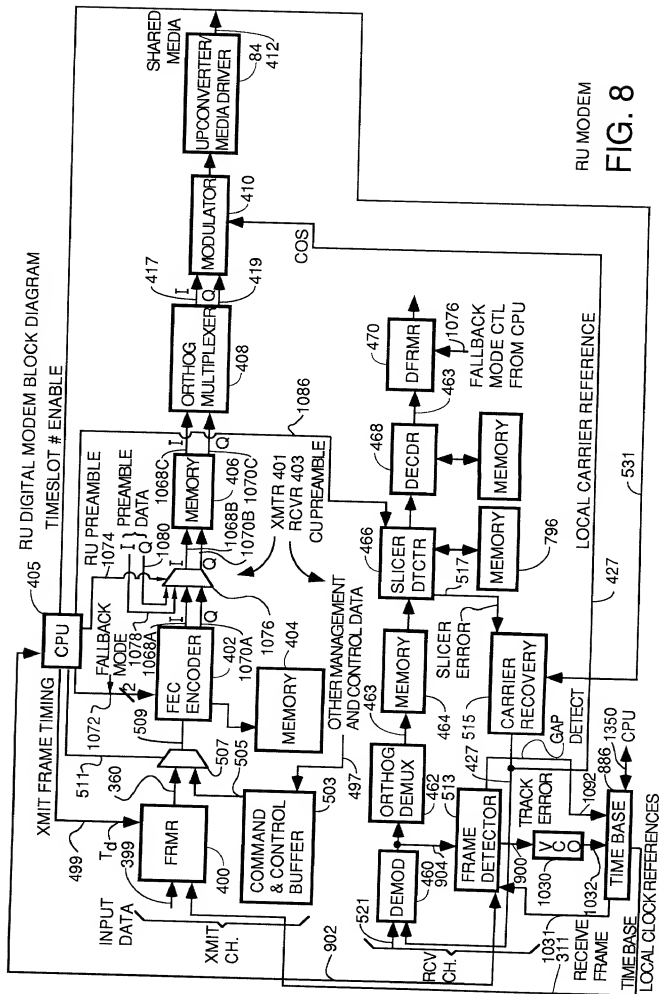


FIG. 7
PRECURSOR EMBODIMENT



RU MODEM

FIG. 8

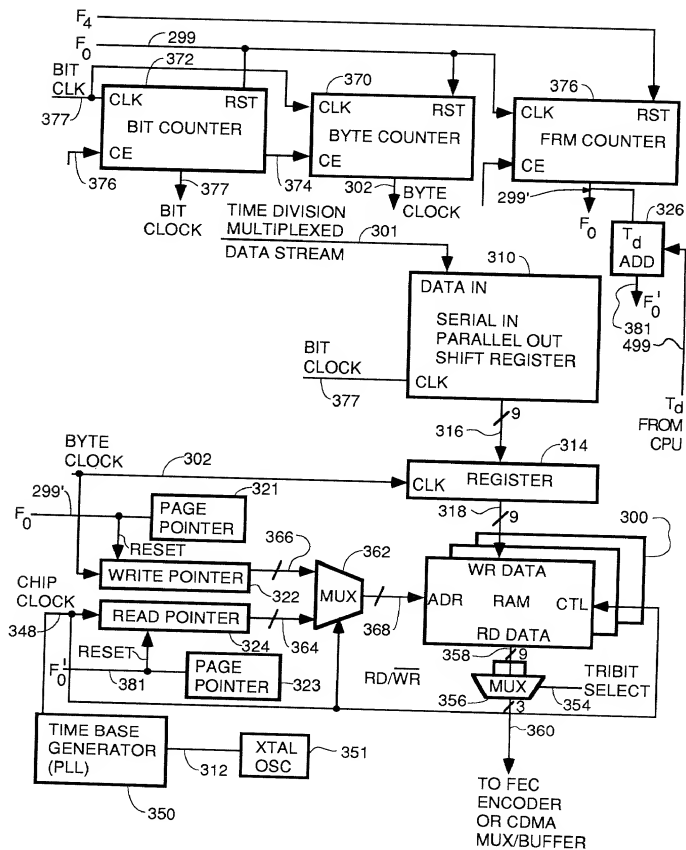


FIG. 9

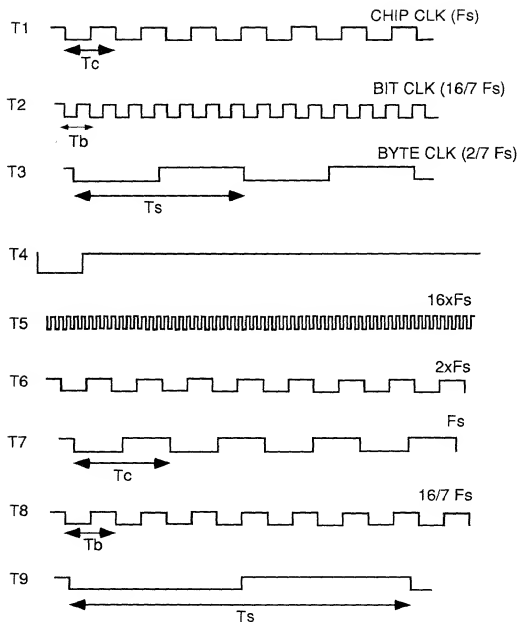


FIG. 10

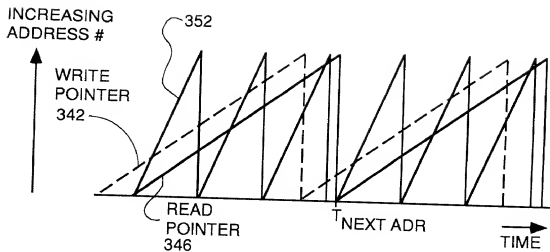


FIG. 15

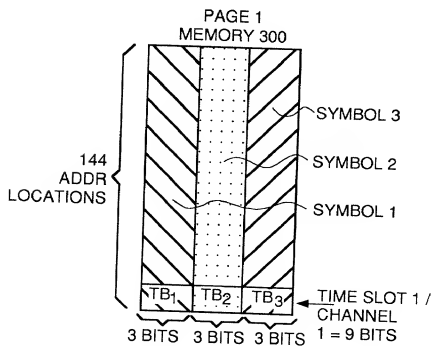
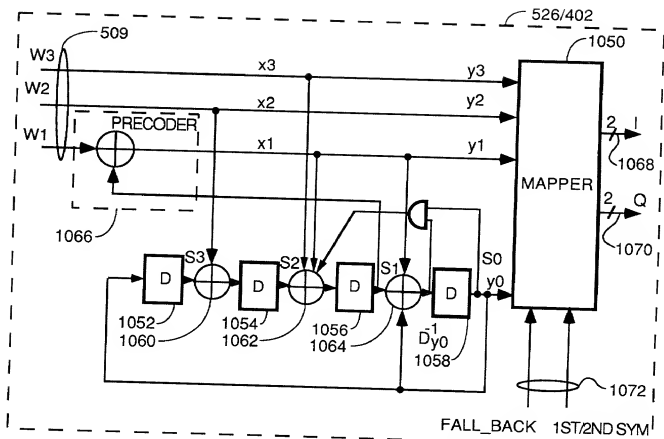


FIG. 16



PREFERRED TRELLIS ENCODER

FIG. 17

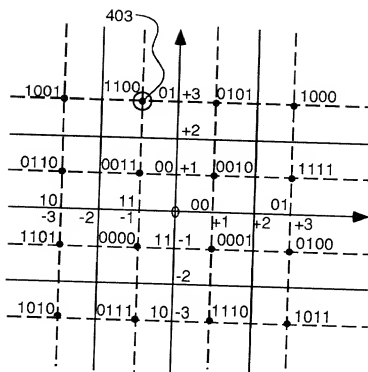


FIG. 18

0000	111	111	
0001	001	111	= 1 - j
0010	001	001	= 1 + j
0011	111	001	= -1 + j
0100	011	111	= 3 - j
0101	001	011	= 1 + 3*j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3*j
1000	011	011	= +3 + 3*j
1001	101	011	= -3 + 3*j
1010	101	101	= -3 - 3*j
1011	011	101	= 3 - 3*j
1100	111	011	= -1 + 3*j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3*j
1111	011	001	= 3 + j

FIG. 19

INFORMATION VECTOR [b] FOR EACH SYMBOL

ORTHOGONAL CODE MATRIX

$$\begin{matrix} 483 \\ 481 \end{matrix} \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ \vdots & & & \end{bmatrix} \times \begin{bmatrix} C_{1,1} & C_{1,2} & \cdots & C_{1,144} \\ C_{2,1} & C_{2,2} & \cdots & C_{2,144} \\ \vdots & \vdots & & \vdots \end{bmatrix}$$

FIG. 20A

REAL PART OF INFO VECTOR [b] FOR FIRST SYMBOL

REAL PART OF RESULT VECTOR

$$\begin{matrix} 405 \end{matrix} \begin{bmatrix} +3 \\ -1 \\ -1 \\ +3 \end{bmatrix} \cdot \begin{matrix} 407 \end{matrix} \begin{bmatrix} 1 & 1 & 1 & 1 \\ -1 & -1 & 1 & 1 \\ -1 & 1 & -1 & 1 \\ -1 & 1 & 1 & -1 \end{bmatrix} = \begin{matrix} 409 \end{matrix} \begin{bmatrix} 4 \\ 0 \\ 0 \\ -8 \end{bmatrix}$$

$[b_{\text{REAL}}] \times [\text{CODE MATRIX}] = [R_{\text{REAL}}] = \text{"CHIPS OUT" ARRAY-REAL}$

FIG. 20B

MAPPING FOR FALL-BACK MODE - LSB'S

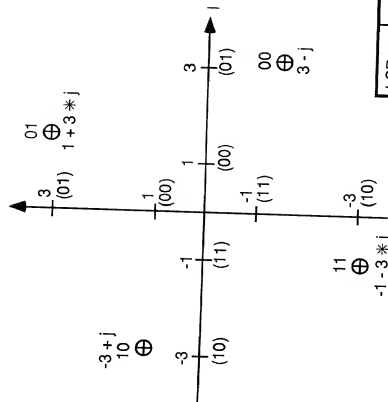


FIG. 21

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+iQ WHEN LSB=00	1+iQ WHEN LSB=01	1+iQ WHEN LSB=10	1+iQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSBs y1 y0	PHASE	1+iQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

LSB & MSB FALLBACK MODE MAPPINGS

FIG. 22

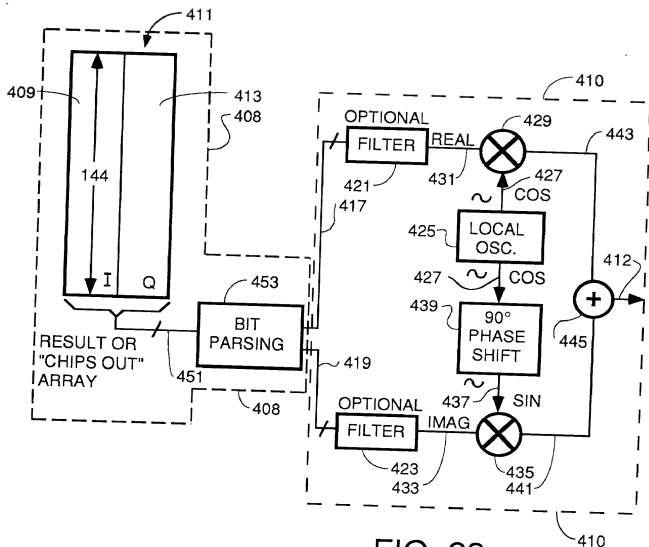


FIG. 23

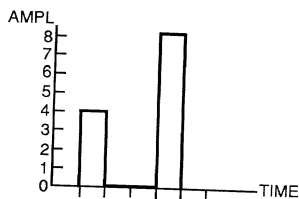


FIG. 24

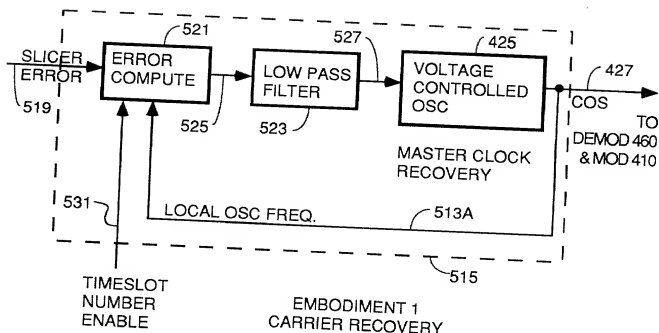


FIG. 25

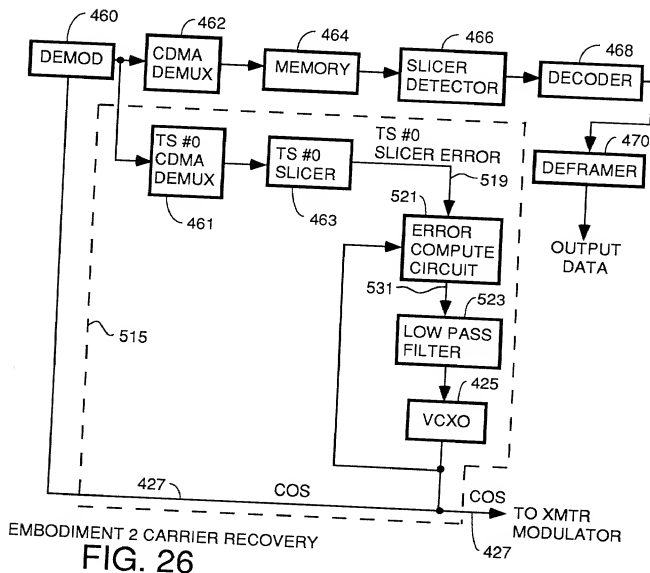


FIG. 26

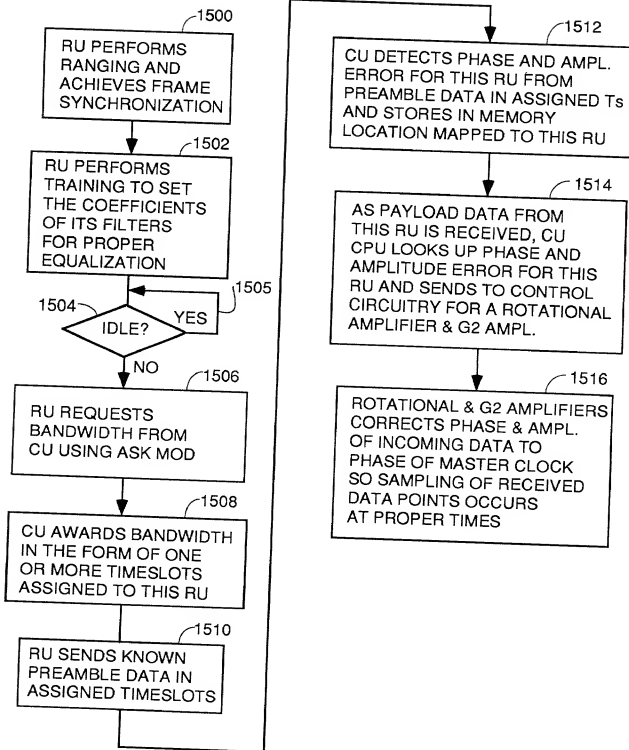
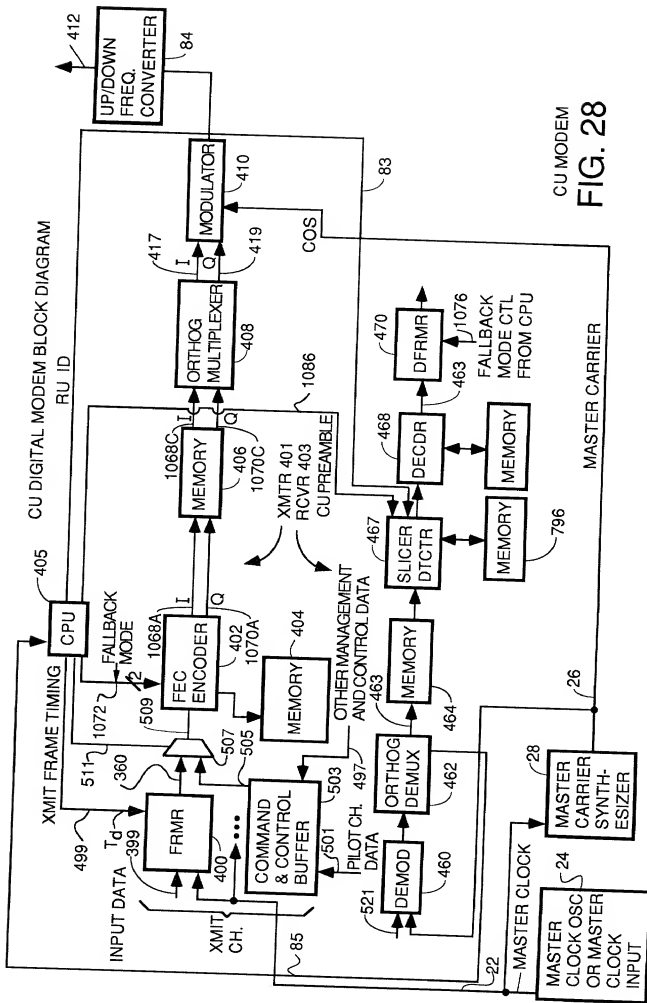


FIG. 27



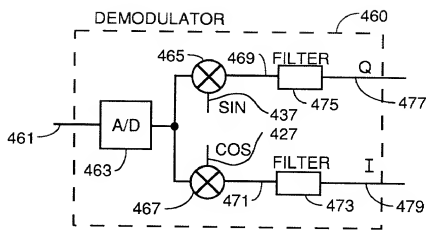
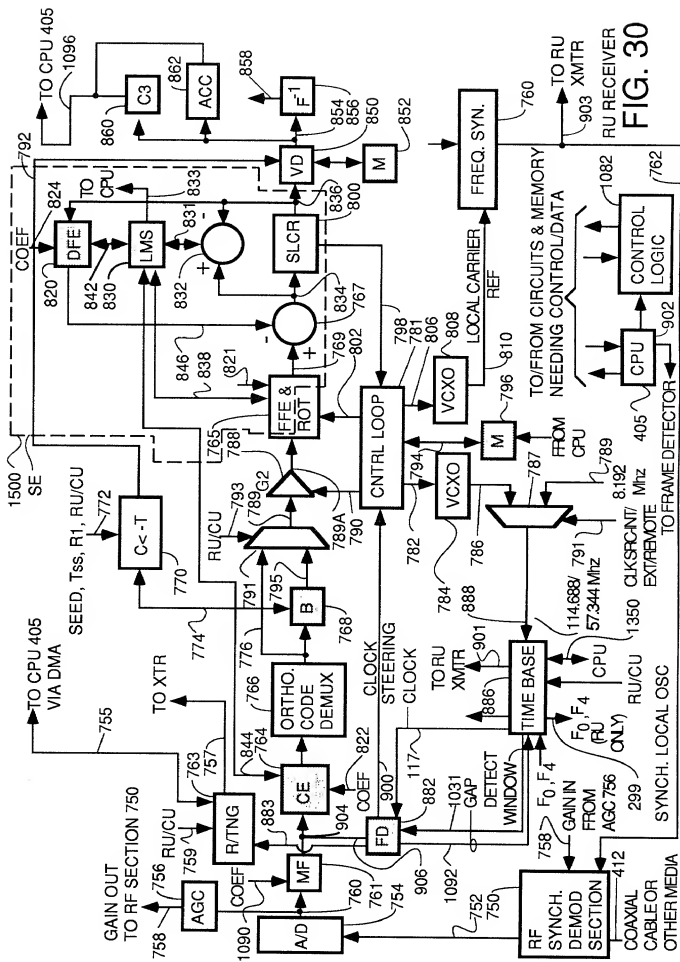
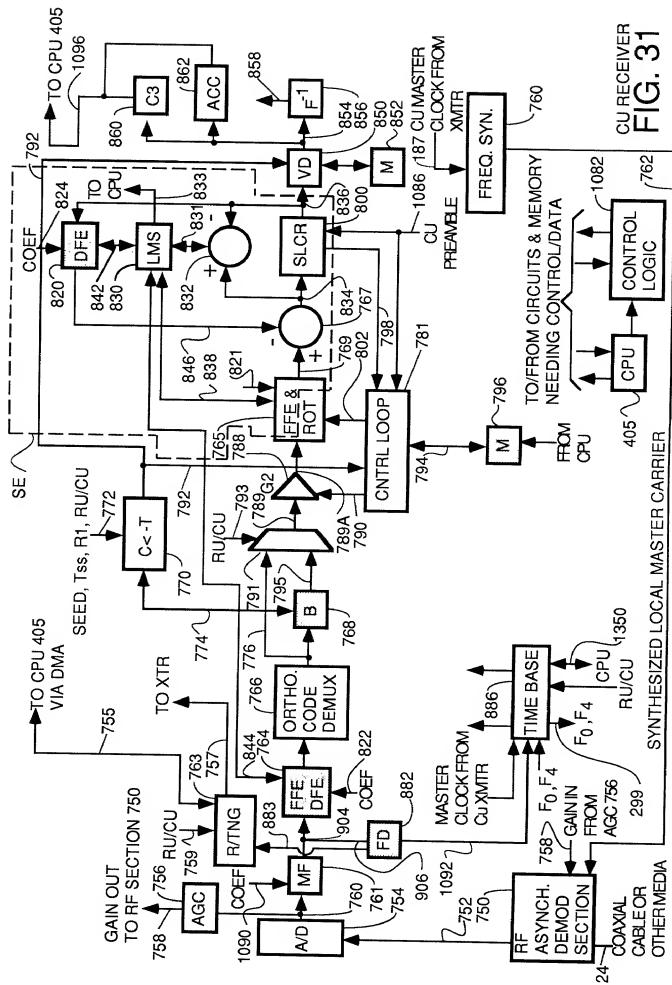
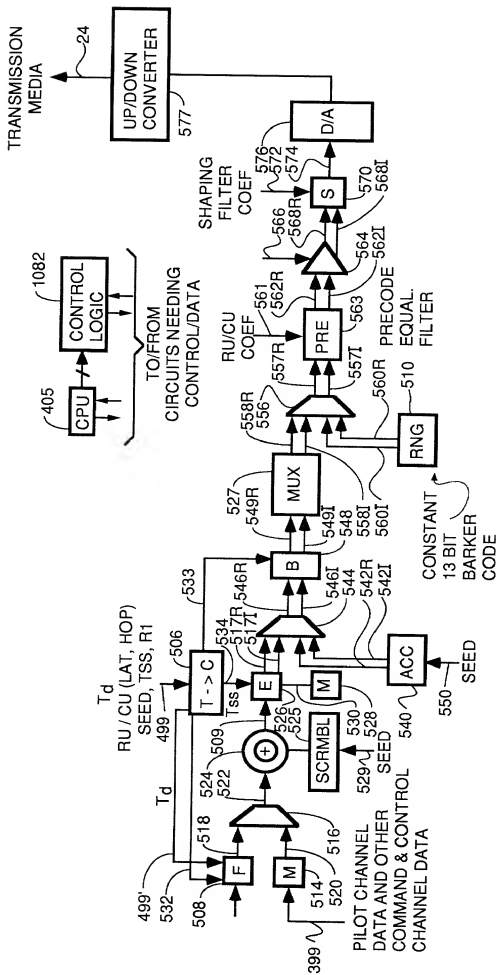


FIG. 29

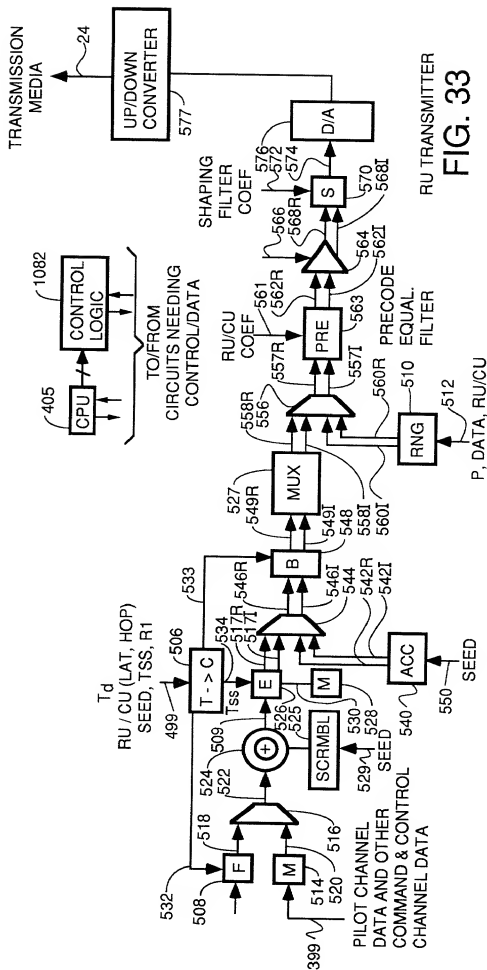


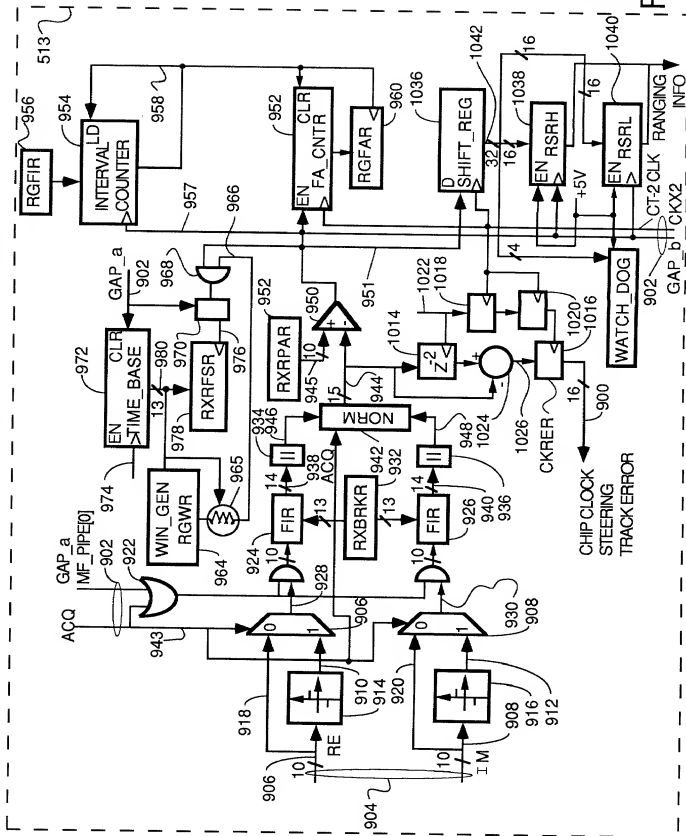




CU TRANSMITTER

FIG. 32





FRAME
DETECTOR
RANGING
DETECTOR

FIG. 34

GAP ACQUISITION TIMING

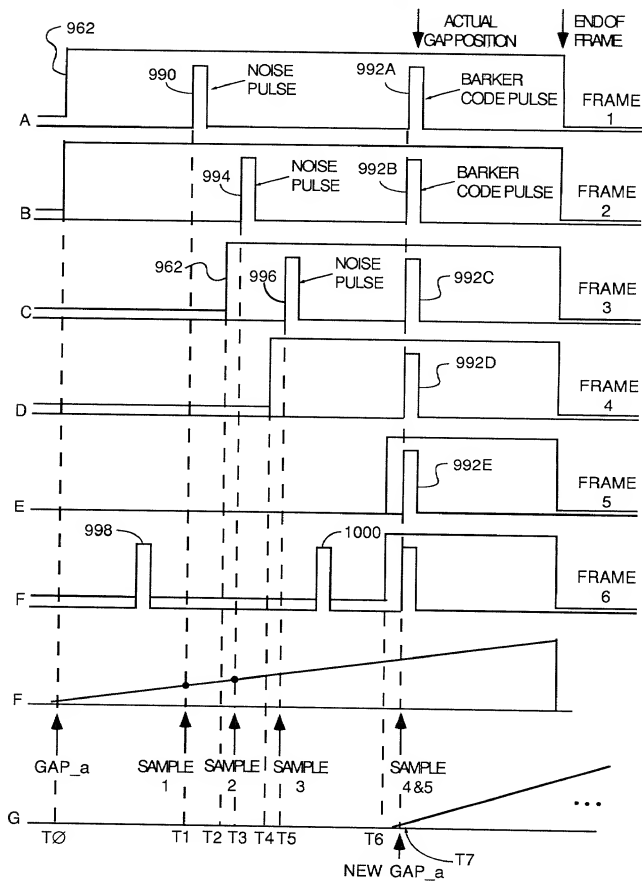


FIG. 35

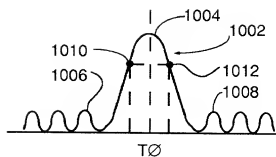


FIG. 36

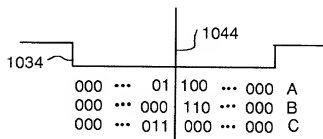


FIG. 37

FINE TUNING TO
CENTER BARKER CODE

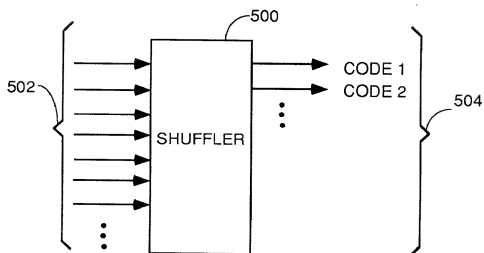


FIG. 38

101250*6E249Z60

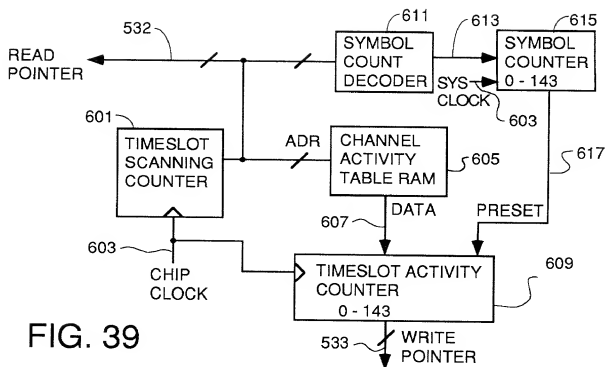


FIG. 39

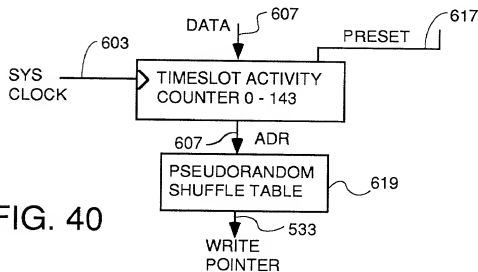


FIG. 40

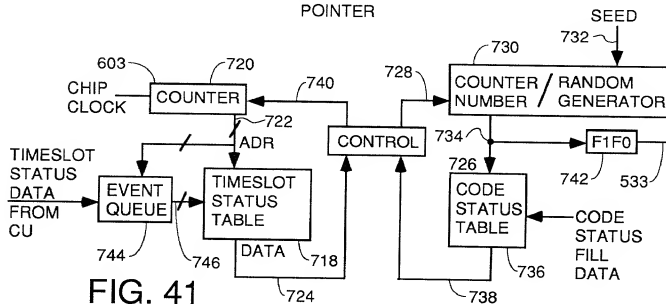


FIG. 41

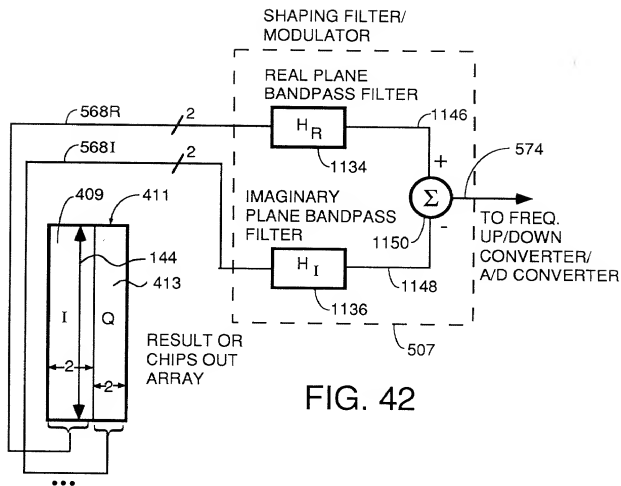


FIG. 42

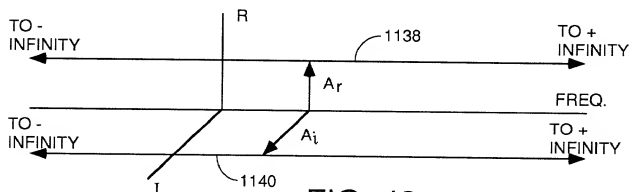


FIG. 43

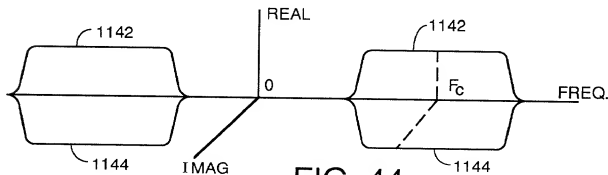
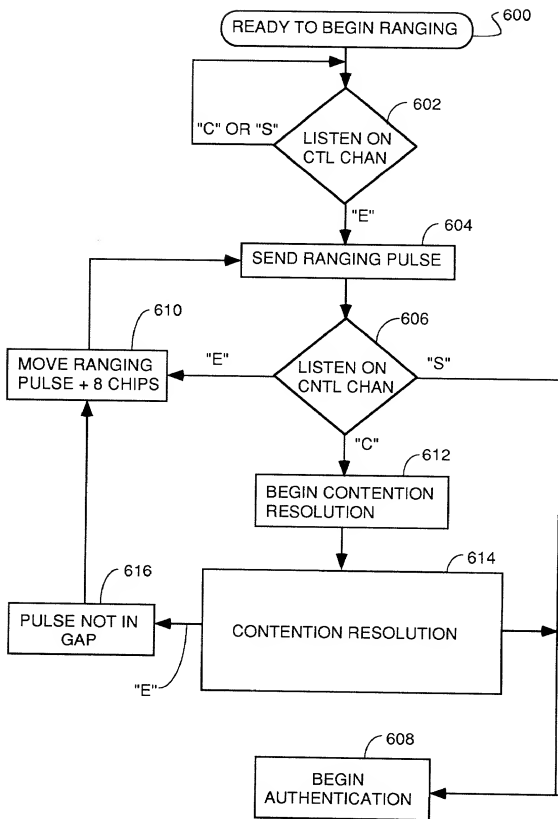
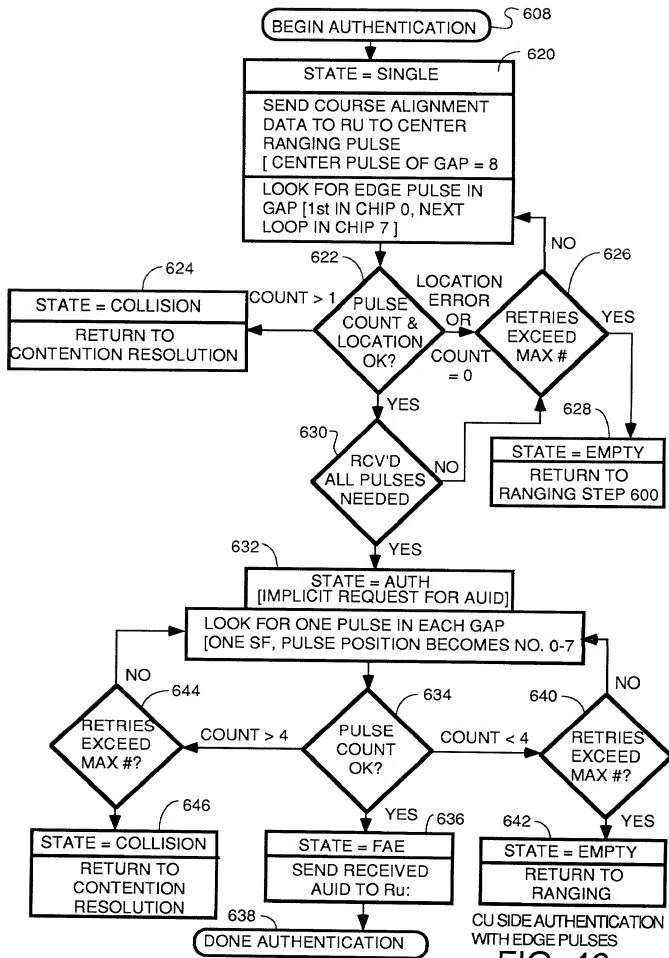


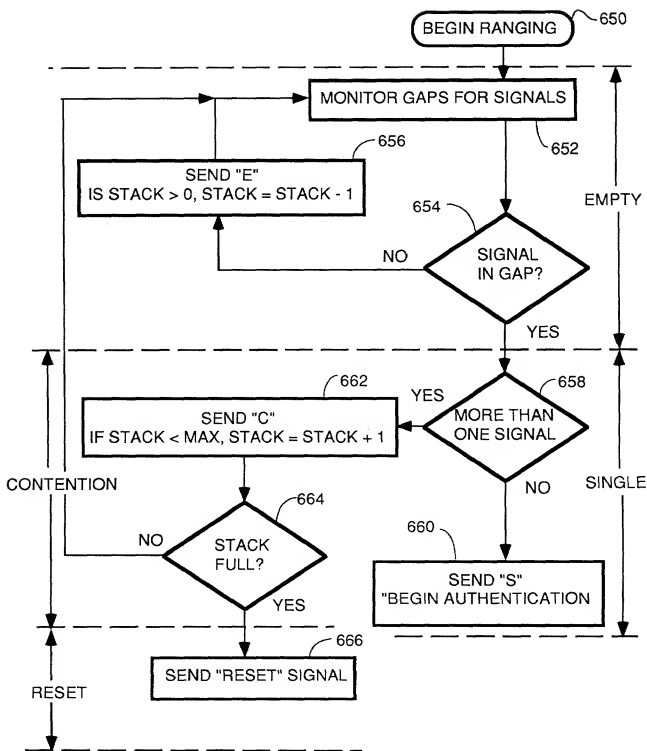
FIG. 44

101250.6249260



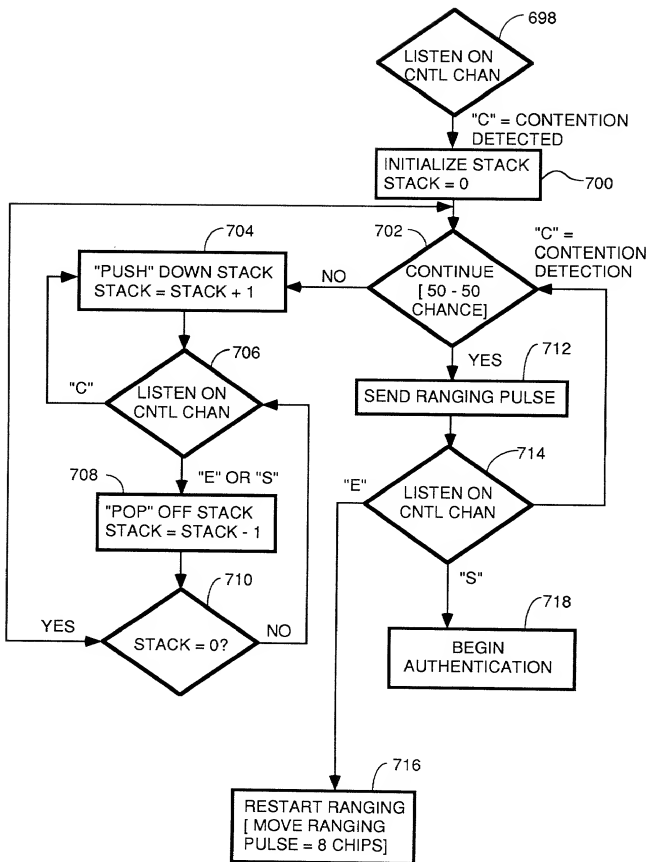
RU RANGING
FIG. 45





CU RANGING AND CONTENTION RESOLUTION

FIG. 47



CONTENTION RESOLUTION - RU
USING BINARY STACK

FIG. 48

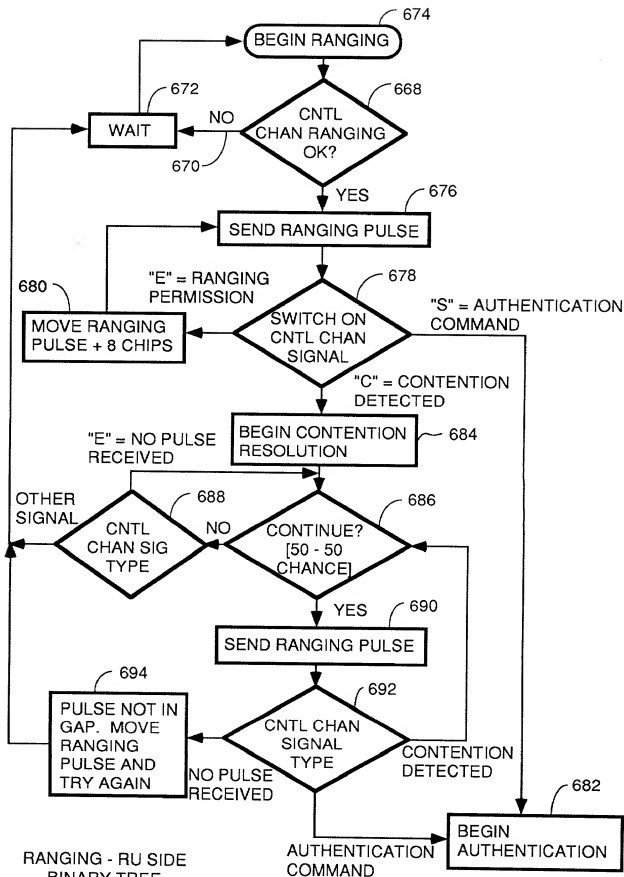


FIG. 49

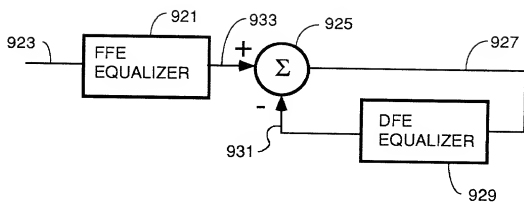


FIG. 50

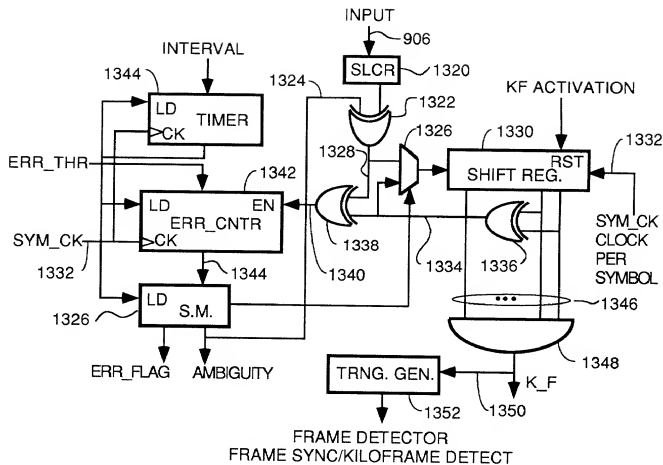
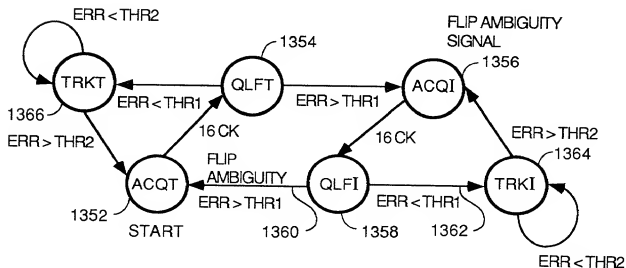


FIG. 51



STATE MACHINE

FIG. 52

09764739 052101

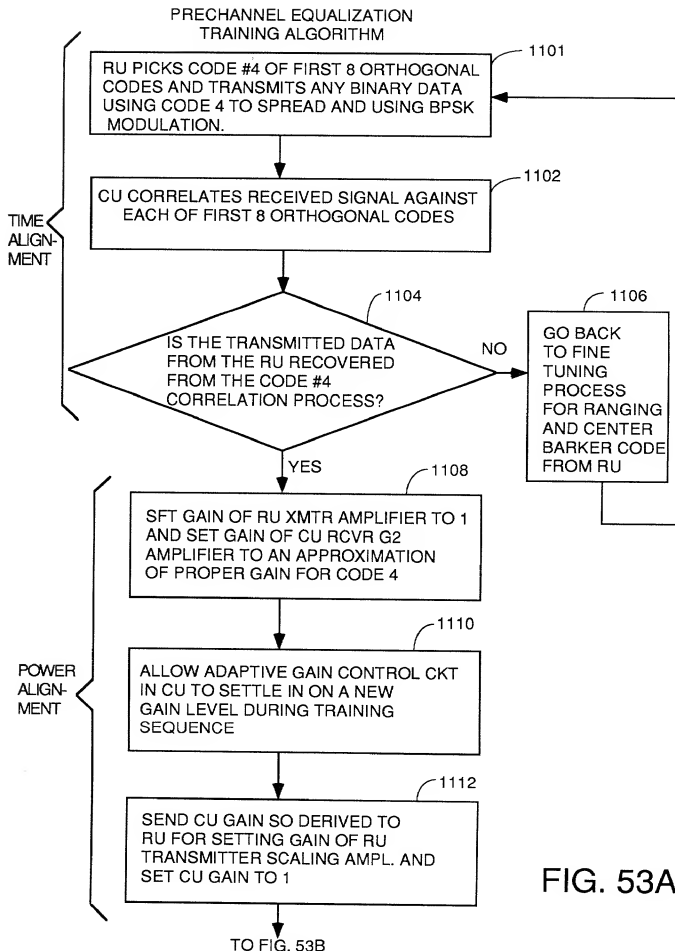


FIG. 53A

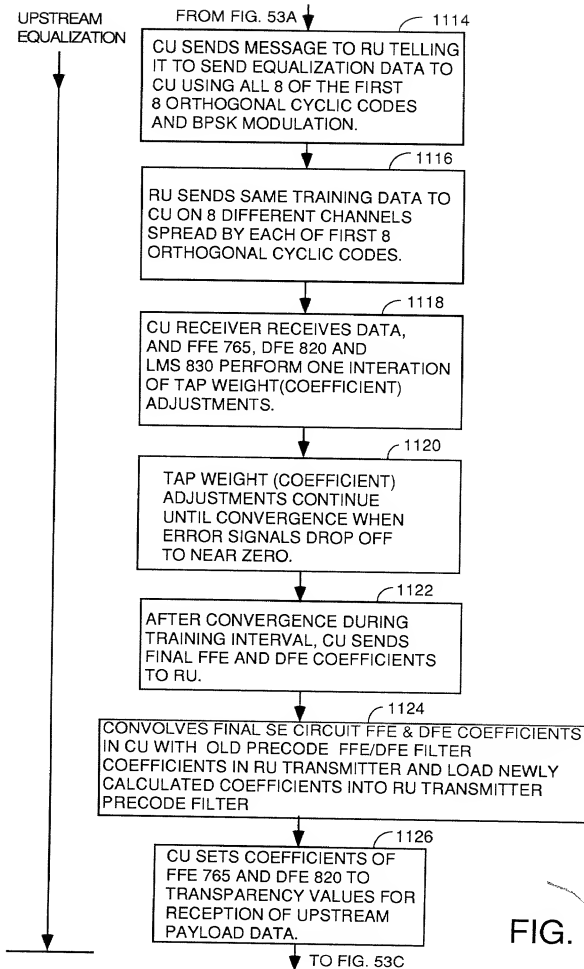


FIG. 53B

DOWNSTREAM
EQUALIZATION

FROM FIG. 53B

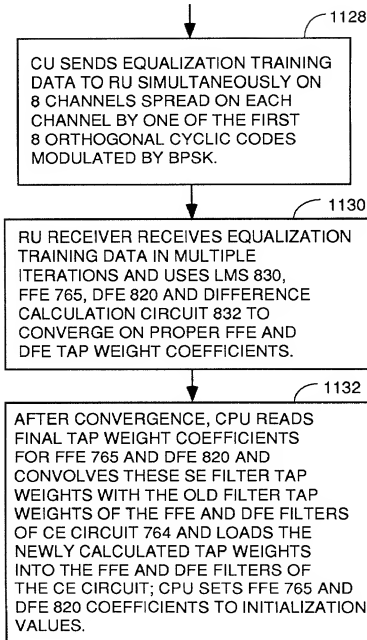


FIG. 53C

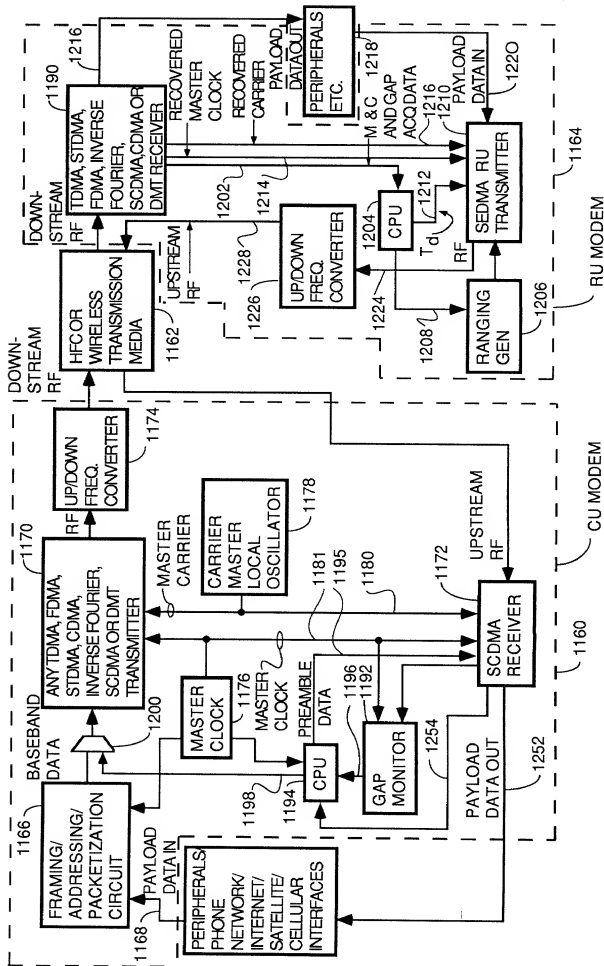
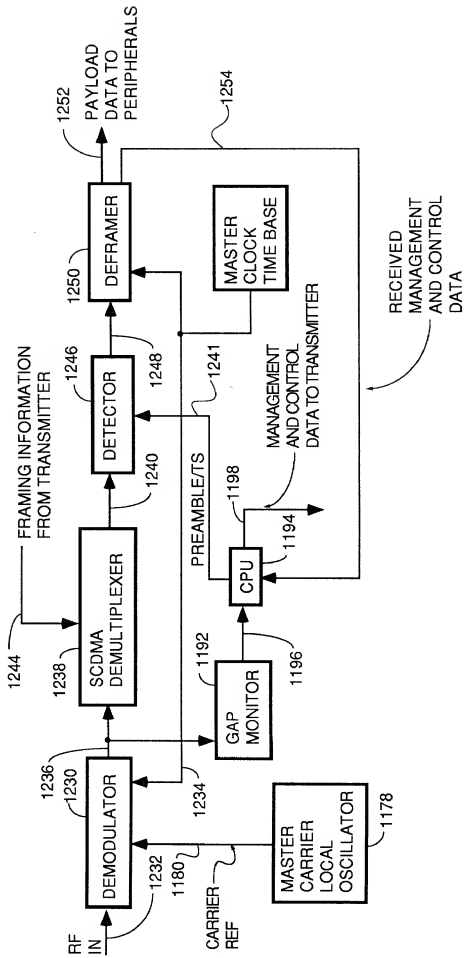


FIG. 54



SIMPLE CU SPREAD SPECTRUM RECEIVER

FIG. 55

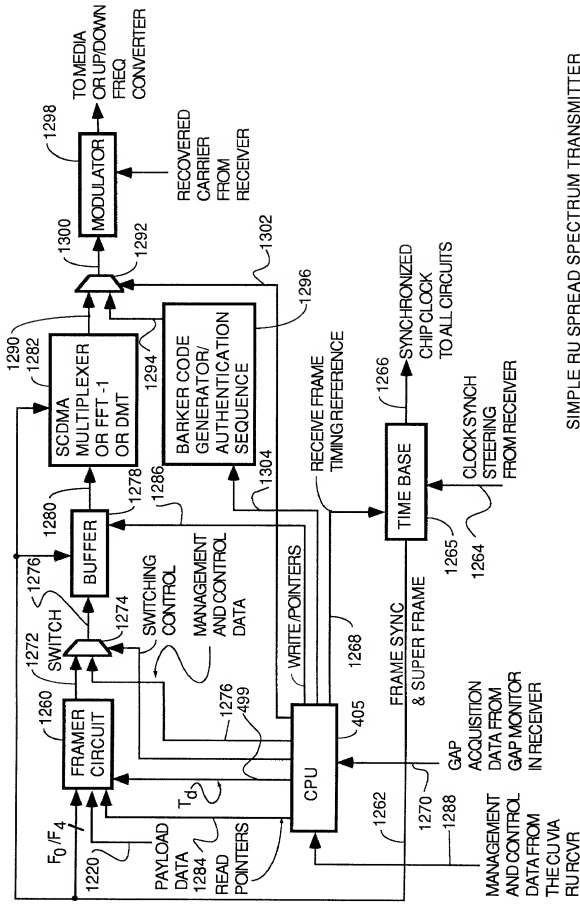
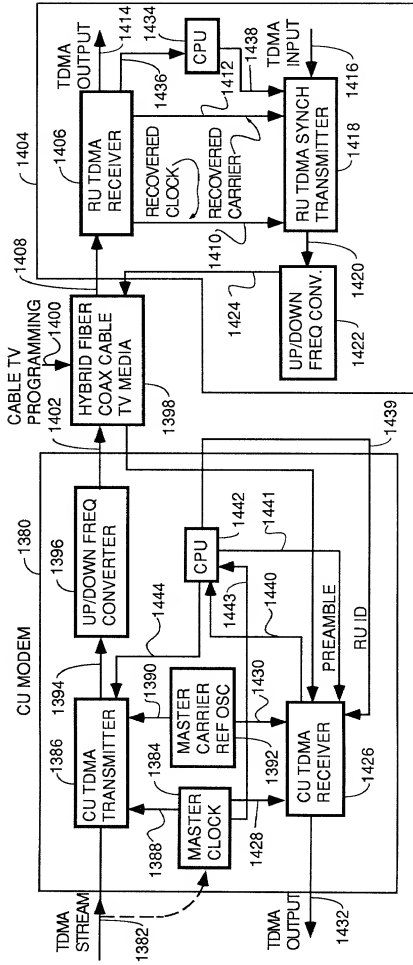


FIG. 56

SIMPLE RU SPREAD SPECTRUM TRANSMITTER



SYNCHRONOUS TDMA SYSTEM

FIG. 57

OFFSET (CHIPS)	1B ASIC		2A ASIC	
	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

TRAINING ALGORITHM

SE FUNCTION

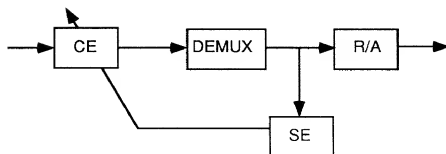
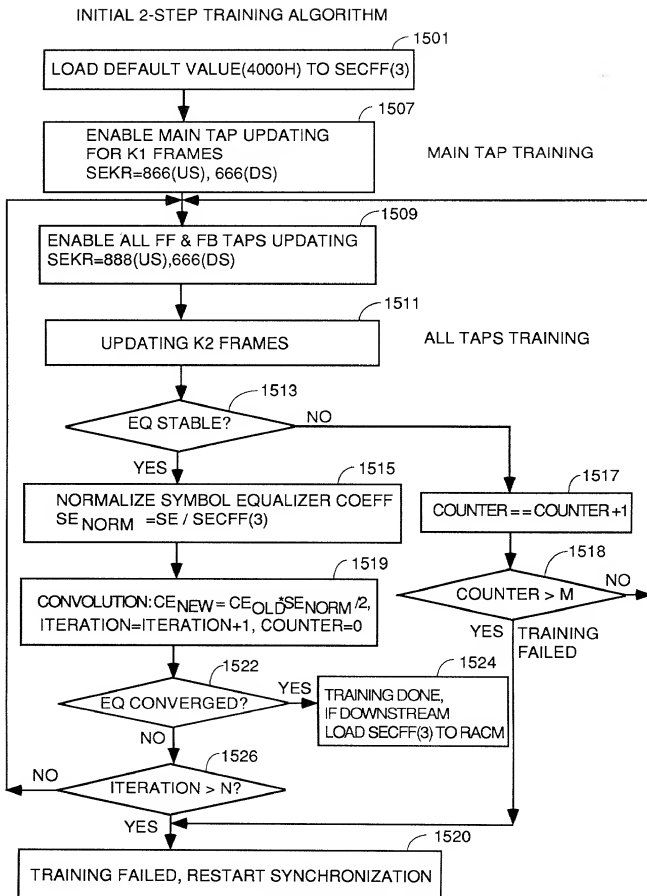


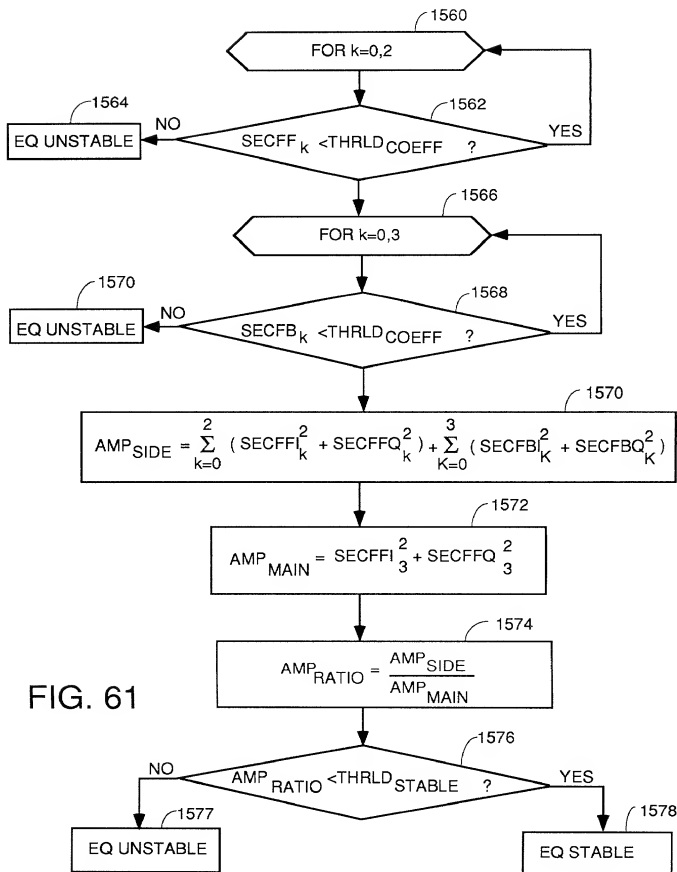
FIG. 59



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

EQ STABILITY CHECK



NOTE: THRLD_{COEFF} = 7F00H

THRLD_{STABLE} = 10⁻³

FIG. 61

PERIODIC 2-STEP TRAINING ALGORITHM

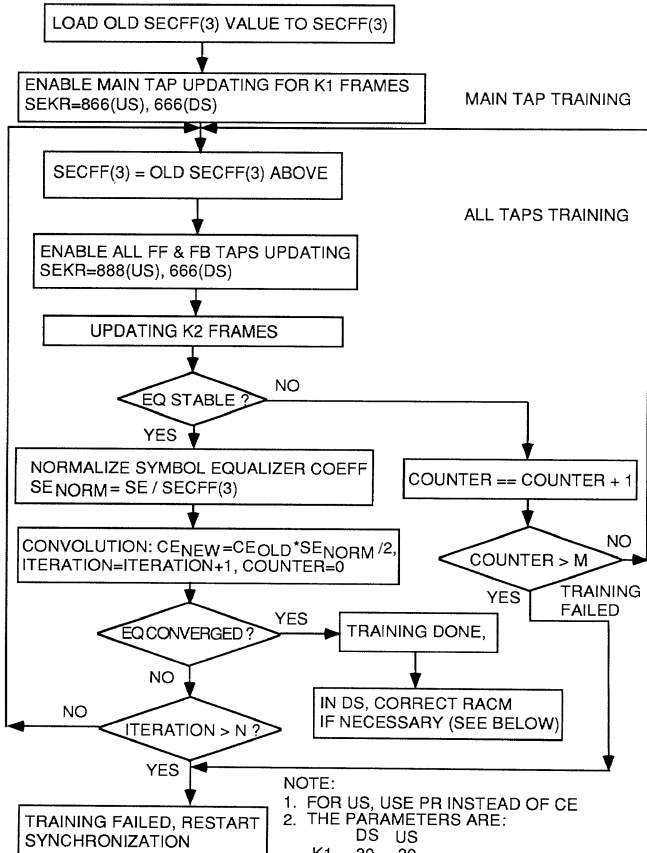
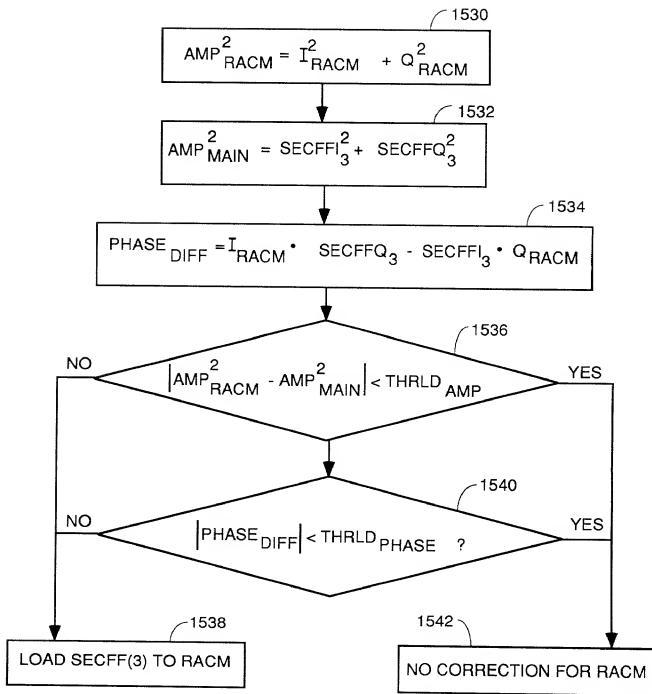


FIG. 62

RACM CORRECTION



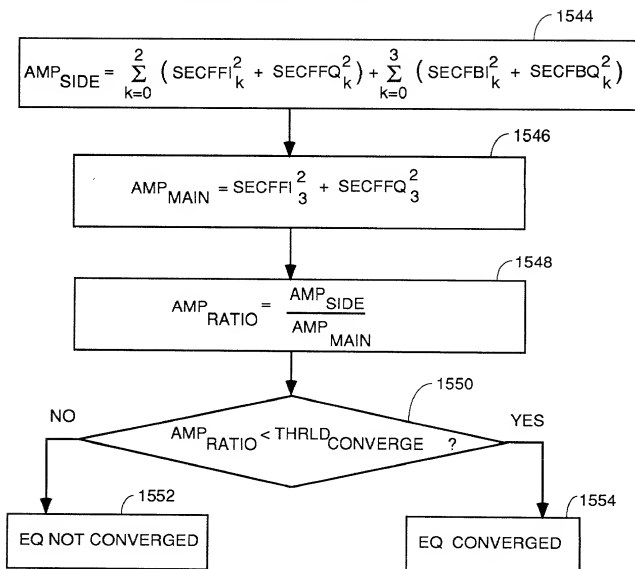
NOTE: $THRLD_{AMP} = TBD$
 $THRLD_{PHASE} = TBD$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

09764739.052101
 101250-64749260

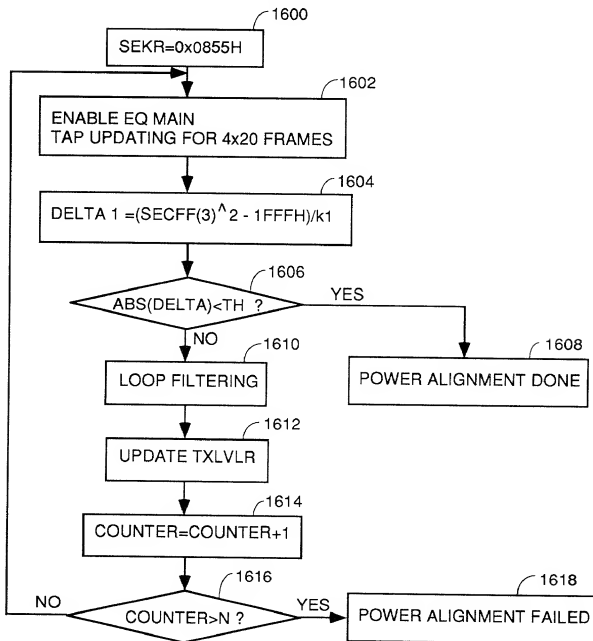
EQ CONVERGENCE CHECK



NOTE: THRLD_CONVERGE = 10⁻⁵

FIG. 64

POWER ALIGNMENT FLOW CHART



NOTE: TH = 600H

N = 12

FIG. 65

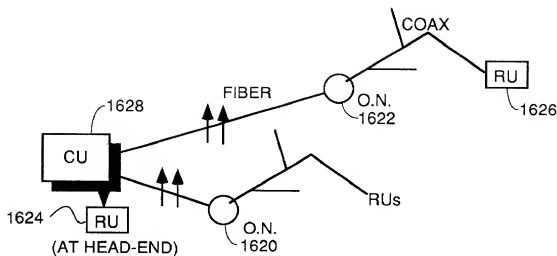
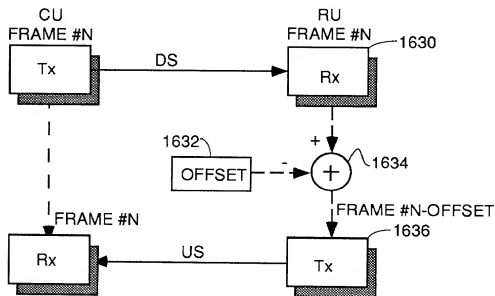


FIG. 66



TOTAL TURN AROUND (TTA) IN FRAMES = OFFSET

FIG. 67

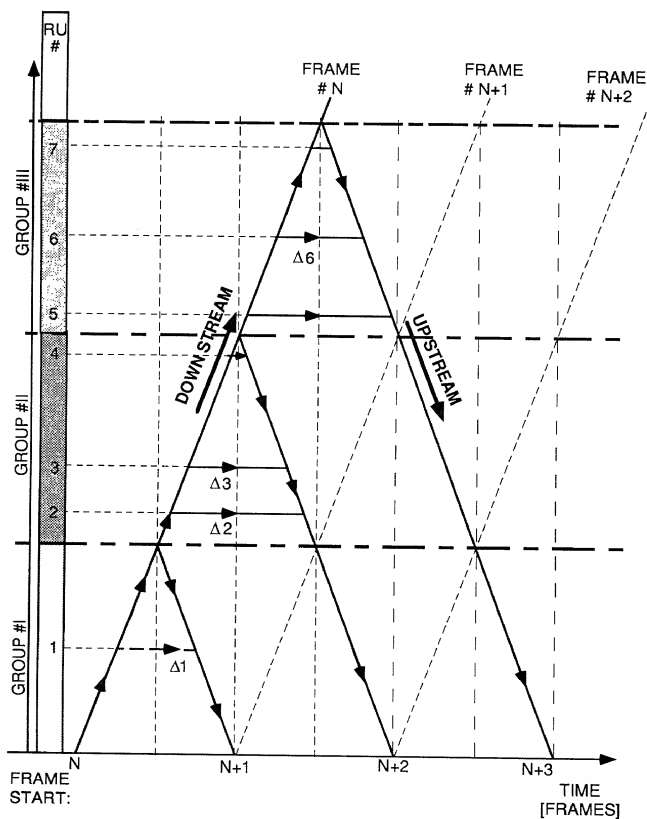
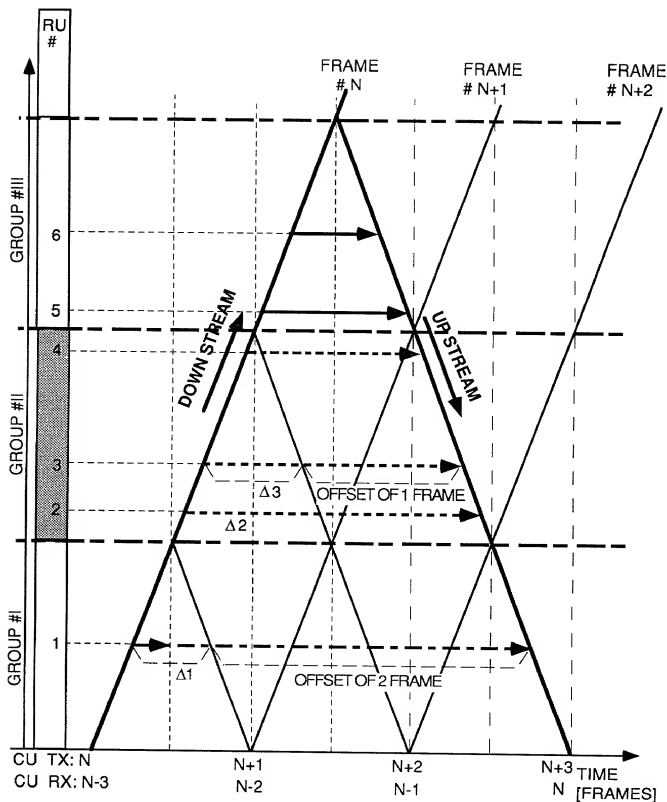


FIG. 68



CONTROL MESSAGE (DOWNSTREAM) AND FUNCTION (UPSTREAM)
PROPAGATION IN A 3 FRAMES TTA CHANNEL

FIG. 69

09764739-052401
101250-5576960

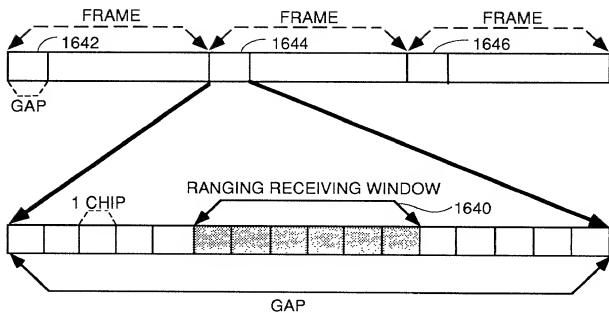
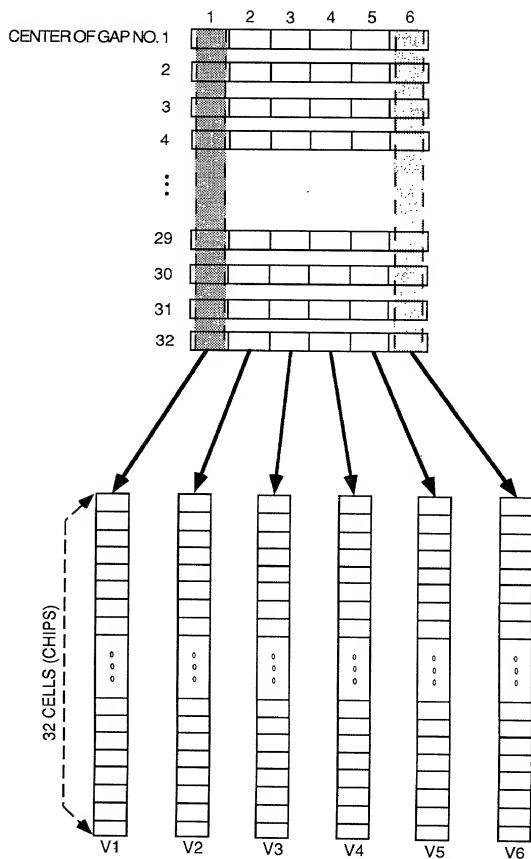


FIG. 70



OVERALL VIEW OF THE CU SENSING WINDOWS
IN A "BOUNDLESS RANGING" ALGORITHM

FIG. 71

CHIP\FR	1	2	3	4	5	6	7		33
1	0	0	1	0	0	1	1	...	0
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72